Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

MCA DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2025

Second Semester

Master of Computer Applications

BX4003/PMCVA103 - Introduction to Computer Organization and Operating Systems

Regulations – 2021/2024

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	What is the function of a Control Unit (CU) in a computer?	L1	1	2
2.	How are instructions represented in machine language?	L2	1	2
3.	What is a basic MIPS implementation, and what are its key components?	L1	2	2
4.	How does a MIPS processor handle exception?	L2	2	2
5.	What are the characteristics and uses of EEPROM (Electrically Erasable Programmable Read-Only Memory)?	L1	3	2
6.	What is the difference between write-through and write-back cache policies?	L2	3	2
7.	Define operating system, and what are its main objectives?	L1	4	2
8.	Write the concept of Process Control Block (PCB) and its role in process management.	L2	4	2
9.	What are the main goals of CPU scheduling?	L1	5	2
10.	Why is fairness an important consideration in CPU scheduling?	L2	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Discuss examples of direct, indirect, register, and immediate addressing modes.	L2	1	8
		ii	Write the purpose of the system clock in a computer.	L2	1	8
			Or			
	b		Explain about logical operations, and why are they essential in a computer's Arithmetic and Logic Unit (ALU)? Discuss common logical	L2	1	16

operations such as AND, OR, XOR, and NOT.

12.	a	i	Discuss the role of the Program Counter (PC) in the MIPS pipeline.	L2	2	8
		i i	Elaborate the purpose of the RegDst and ALUOp signals in MIPS control implementation?	L2	2	8
			Or			
	b		Describe the five stages of the MIPS pipeline (IF, ID, EX, MEM, and WB). How does each stage perform its respective task, and how does the pipelining process affect the overall performance of the processor?	L2	2	16
13.	a		Explain the trade-offs between fast but small memory (e.g., registers and cache) and large but slower memory (e.g., main memory and secondary storage). Why is it important to use multiple levels of memory in modern computer systems?	L3	3	16
			Or			
	b		Explain how a DMA controller works to manage data transfer between I/O devices and memory. Describe the role of the DMA controller in generating memory access requests.	L3	3	16
14.	a		Describe the evolution of operating systems from early batch systems to modern multiprogramming and time-sharing systems. What were the major milestones in the development of OS?	L3	4	16
			Or			
	b		Discuss the different states of a process (e.g., new, ready, running, waiting, terminated). How does the operating system manage processes in each of these states?	L3	4	16
15.	a		You are designing an operating system for a real-time embedded system where task deadlines are crucial. The system has tasks with varying burst times, and some tasks need to complete before a certain time to ensure system reliability. Which CPU scheduling algorithm would you choose for this system, and why? How would it affect the system's performance in terms of meeting task deadlines?	L4	5	16
			Or			
	b		You are implementing a real-time control system where multiple processes need to access shared memory to update system parameters. However, there is a risk of data inconsistency due to simultaneous access. How would you manage critical sections in this real-time system? Which synchronization tools (e.g., locks, semaphores) would you use to ensure data integrity?	L4	5	16